IN THE CLAIMS

Please amend the claims as indicated below.

1. (currently amended) A field transistor containing no thin gate insulating layer comprising:

a well region of a first conductivity type;

a field oxide layer for defining an active region on the well region;

high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer;

a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer;

a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and

a gate conductive layer pattern formed on the field oxide layer, the gate conductive layer pattern overlapping parts of the low concentration source and drain regions of the second conductivity type.

2. (original) The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a high concentration buried region of the first conductivity type on a semiconductor substrate of the first conductivity type.

3. (previously presented) The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a semiconductor substrate of the first conductivity type.

4. (original) The field transistor of claim 1, further comprising a high concentration diffusion region of the first conductivity type formed in the well region, the high concentration diffusion region being separated from the high concentration source region of the second conductive type by a predetermined distance.

5. (original) The field transistor of claim 4, further comprising a low concentration diffusion region of the first conductivity type and a low concentration diffusion region of the

second conductivity type, both low concentration diffusion regions being adjacent to each other between the high concentration diffusion region of the first conductivity type and the high concentration source region of the second conductivity type.

6. (original) The field transistor of claim 5, wherein the low concentration diffusion region of the first conductivity type is adjacent to the high concentration diffusion region of the first conductivity type, and the low concentration diffusion region of the second conductivity type is adjacent to the high concentration source region of the second conductivity type.

7. (original) The field transistor of claim 1, further comprising:

a gate electrode electrically connected to the gate conductive layer pattern;

a source electrode electrically connected to the high concentration source region of the second conductivity type; and

a drain electrode electrically connected to the high concentration drain region of the second conductivity type.

8. (original) The field transistor of claim 7, wherein the drain electrode is electrically connected to the gate electrode.

9. (original) The field transistor of claim 7, wherein the source electrode is electrically connected to the high concentration diffusion region of the first conductivity type as well.

10. (original) The field transistor of claim 1, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

11. (withdrawn) A method of manufacturing a field transistor comprising the steps of:

sequentially forming an oxide layer and a mask layer pattern on a well region of a first conductivity type;

using the mask layer pattern as an ion implantation mask to implant impurity ions of the first conductivity type into the well region;

forming a photoresist layer pattern on portions of the oxide layer and the mask layer pattern;

using the exposed portion of the mask layer pattern and the photoresist layer pattern as an ion implantation mask to implant impurity ions of a second conductivity type into the well region;

removing the photoresist layer pattern;

forming a field oxide layer in which a portion of the oxide layer is grown using the mask layer pattern as an oxide growth prevention layer while diffusing the impurity ions of the first and second conductivity types to form low concentration source/drain regions of the second conductivity type;

forming high concentration source/drain regions of the second conductivity type on either side of the field oxide layer in the well region;

forming a high concentration diffusion region of the first conductivity type so that the high concentration diffusion region of the first conductivity type is separated from the high concentration source region of the second conductivity type by a predetermined distance; and

forming a gate conductive layer pattern on the field oxide layer.

12. (withdrawn) The method of claim 11, wherein the photoresist layer pattern exposes the oxide layer corresponding to a portion of the well region into which the impurity ions of the first conductivity type are implanted.

13. (withdrawn) The method of claim 11, wherein the implantation concentration of the impurity ions of the second conductivity type is higher than that of the impurity ions of the first conductivity type.

14. (withdrawn) The method of claim 11, wherein the gate conductive layer pattern overlaps the low concentration source/drain regions of the second conductivity type by interposing the field oxide layer therebetween.

15. (withdrawn) The method of claim 11, further comprising the steps of:

forming a gate electrode so that the gate electrode is electrically connected to the gate conductive layer pattern;

forming a source electrode so that the source electrode is electrically connected to the high concentration source region of the second conductivity type; and

forming a drain electrode so that the drain electrode is electrically connected to the high concentration drain region of the second conductivity type.

16. (withdrawn) The method of claim 15, wherein the drain electrode is electrically connected to the gate electrode.

17. (withdrawn) The method of claim 15, wherein the source electrode is electrically connected to the high concentration diffusion region of the first conductivity type.

18. (withdrawn) The method of claim 11, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

19. (currently amended) A semiconductor device containing no thin gate insulating layer, comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over a portion of the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

20. (original) The device of claim 19, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region.

21. (original) The device of claim 20, further comprising a second diffusion region having a first conductivity type concentration lower than the first diffusion region and comprising a third diffusion region of the second conductivity type, both the second and third diffusion regions adjacent each other and located between the first diffusion region and the first source region.

22. (original) The device of claim 21, the second diffusion region type located adjacent the first diffusion region and the third diffusion region located adjacent the first source region.

23. (original) The device of claim 19, further comprising:

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

24. (original) The device of claim 23, the drain electrode being electrically connected to the gate electrode.

25. (original) The device of claim 23, the source electrode being electrically connected to the first diffusion region.

26. (original) The device of claim 19, wherein the first conductivity type is p-type and the second conductivity type is n-type.

27. (currently amended) A semiconductor device containing no thin gate insulating layer, comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer;

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region;

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

28. (original) The device of claim 27, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region, a second diffusion region having a first conductivity type concentration lower than the first diffusion region, and a third diffusion region of the second conductivity type, wherein both the second and third diffusion regions are adjacent each other and located between the first diffusion region and the first source region.

29. (currently amended) A system for electrostatic discharge protection containing a field transistor without a thin gate insulating layer, the field transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

30. (withdrawn) A method for making a semiconductor device, comprising:

providing a substrate containing a well region of a first conductivity type;

providing a field oxide layer over a portion the well region;

providing a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

providing a second source region having a second conductivity type concentration lower than the first source region, the second source region provided in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

providing a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region provided in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

providing a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

31. (withdrawn) The method of claim 30, further including:

providing a gate electrode electrically connected to the conductive layer;

providing a source electrode electrically connected to the first source region; and

providing a drain electrode electrically connected to the first drain region.

32. (withdrawn) The method of claim 30, further including:

providing a first diffusion region of the first conductivity type in the well region and separated from the first source region;

providing a second diffusion region having a first conductivity type concentration lower than the first diffusion region; and

providing a third diffusion region of the second conductivity type;

the second and third diffusion regions being provided adjacent each other and located between the first diffusion region and the first source region.

33. (withdrawn) A method for making a semiconductor device, comprising:

providing a well region of a first conductivity type in a substrate;

providing an oxide layer and a patterned mask layer on the well region;

implanting ions of the first conductivity type into the well region using the mask layer as an ion implantation mask;

providing a patterned photoresist layer on a portion of the oxide layer and the mask layer;

implanting ions of the second conductivity type into the well region using the exposed portion of the mask layer and the photoresist layer as an ion implantation mask;

removing the photoresist layer;

providing a field oxide layer using the mask layer to prevent oxide growth while diffusing the ions of the first and second conductivity types;

providing first source and drain regions of the second conductivity type on either side of the field oxide layer;

providing a diffusion region of the first conductivity type separate from the first source region; and

providing a patterned gate conductive layer over the field oxide layer.

34. (withdrawn) The method of claim 33, wherein the photoresist layer exposes the oxide layer corresponding to the portion of the well region into which the ions of the first conductivity type are implanted.

35. (withdrawn) The method of claim 33, wherein the concentration of the ions of the second conductivity type is higher than that of the ions of the first conductivity type.

36. (withdrawn) The method of claim 33, further including:

forming a gate electrode to be electrically connected to the gate conductive layer;

forming a source electrode to be electrically connected to the first source region; and

forming a drain electrode to be electrically connected to the first drain region.

37. (withdrawn) The method of claim 36, including electrically connecting the drain electrode to the gate electrode.

38. (withdrawn) The method of claim 36, including electrically connecting the source electrode to the diffusion region.

39. (withdrawn) The method of claim 33, wherein the first conductivity type is p-type and the second conductivity type is n-type.

40. (original) A semiconductor device for electrostatic discharge protection, the device comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer while containing no gate insulating layer.

41. (original) A system for electrostatic discharge protection, the system comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer while containing no gate insulating layer.